UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,237	08/23/2001	Dale T. Platteter	D/A0A73	1681

7590 06/09/2004

Patrick R. Roche
Fay, Sharpe, Fagan
Minnich & McKee, LLP
1100 Superior Avenue, 7th Floor
Cleveland, OH 44114-2518

EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	3

DATE MAILED: 06/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,237	PLATTETER ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on August 23, 2001 was filed before the mailing date of the first Office Action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

2. Claims 1, 6, and 9 are objected to because of the following informalities:

- As per claim 1, "discrete interrupt signal" on lines 5 and 7 should be "discrete clock synchronization interrupt signal" in order to correspond with the antecedent established on lines 2-3;
- As per claim 6, the "clock synchronization interrupt signal" and "interrupt signal" on lines 26-7 and 28 respectively should be "discrete clock synchronization interrupt signal" in order to correspond with the antecedent established in claim 1; and
- As per claim 9, "the resource and the controller" on line 10 should be "the *resources* and the controller".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3, 6-7, 10-11, and 21 rejected under 35 U.S.C. 102(b) as being anticipated by Yamanaka et al., U.S. Patent 4807259, hereinafter Yamanaka.

5. These rejections are supported by the following fact findings:

Findings for 102

5.1. Yamanaka discloses a document processing system [master station 1 comprises typewriter 13 for document processing][1].

5.2. The system comprises a controller [master station 1], including a master clock [17] and logic [CPU 10 and code sending and receiving circuit 18] for generating a discrete clock synchronization interrupt signal [S11; col.7, ll.6-8; being utilized in a synchronization process, S11 is an interrupt signal requiring the receiving station to act on the signal within an acceptable time of tp – col.7, ll.17-20].

5.3. The system comprises a resource [slave station 2], including a slave clock [27] related to operational timing of the resource [the slave station utilizes a slave clock to provide timing functionality to slave station components such as CPU 20 which inherently, requires a local timing input] and circuitry for receiving and processing the discrete clock synchronization interrupt signal [code sensing and receiving circuit 28 and CPU 20; col.3, ll.5-11; col.7, ll.12-17].

5.4. The system comprises a control bus [data transmission path 5], interconnecting the resource and the controller, for distributing the discrete interrupt signal [col.2, ll.25-28; col.4, ll.20-22].

---

[1] Although there are several embodiments, the pertinent reference items generally have the same functionalities and do not contradict one another [col.6, ll.37-41, ll.53-55].

5.5. The resource circuitry includes a processor [CPU 20] for adjusting the slave clock to provide for compatibility with the controller [col.7, ll.42-47].

5.6. The system includes a plurality of resources [slave stations 2 and 3], each resource including a slave clock [27 and 37] related to operational timing of the resource and circuitry for receiving and processing the clock synchronization interrupt signal [code sending and receiving circuit 28 and 38, CPU 20 and 30].

5.7. The control bus [data transmission path 5] interconnects each resource with the controller thereby distributing the interrupt signal to each resource [col.2, ll.25-28; col.4, ll.20-22].

5.8. The circuitry in each resource includes a processor [CPU 20 and 30] for adjusting the slave clock associated with the resource to provide for compatibility with the controller [col.7, ll.42-47].

5.9. The system comprises a plurality of resources [slave stations 2 and 3], each resource including a slave clock [27 and 37] related to operational timing of the resource and logic for receiving the discrete interrupt signal [code sending and receiving circuit 28 and 38], processing the discrete interrupt signal [CPU 20 and 30], and synchronizing the slave clock with the master clock [col.7, ll.42-47].

5.10. The system comprises electrical wiring [data transmission path 5] interconnecting the resources and the controller for distributing the discrete interrupt signal to the resources [col.2, ll.25-28; col.4, ll.20-22].

5.11. Yamanaka discloses the resources include one or more finishing devices [output circuit 24].

5.12. Yamanaka discloses the resources include one or more feeding devices [input circuit 25].

Re Claim 1, 3, 6-7, 10-11, and 21

6. In re claim 1, Yamanaka teaches each and every limitation as set forth in findings 5.1-5.4.

7. As to claim 3, see finding 5.5.

8. As to claim 6, see findings 5.6 and 5.7.

9. As to claim 7, see finding 5.8.

10. As to claim 10, see finding 5.11.

11. As to claim 11, see finding 5.12.

12. As to claim 21, see findings 5.2, 5.9 and 5.10.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. The following are fact findings for claims 2, 4-5, 8-9, and 12-20:

Findings for 103

14.1. Yamanaka discloses a document processing system comprising a plurality of resources [slave stations 2 and 3] [col.7, ll.3-5].

14.2. Yamanaka discloses a method of initially synchronizing the slave clock with the master clock [abstract].

14.3. Yamanaka discloses the method comprising saving a value of the master clock in the controller [col.7, ll.9-11].

14.4. Yamanaka discloses the method comprising generating a discrete clock synchronization interrupt signal in the controller and distributing the discrete interrupt signal to the resource via the control bus [col.7, ll.6-8].

14.5. Yamanaka discloses the method comprising receiving the discrete interrupt signal at the resource and saving a first value of the slave clock [col.7, ll.12-17].

14.6. Yamanaka teaches the advantage of synchronizing the master and slave clocks within a range of error in order to avoid problems for practical use [col.1, ll.56-59].

14.7. Cheung et al., U.S. Patent 5535217, hereinafter Cheung, discloses a system for synchronizing a master and slave clocks [col.1, ll.8-12].

14.8. Cheung discloses the resource circuitry includes a processor [CPU 202] for determining the compatibility of the slave clock with the master clock [FIG.12; col.3, ll.2-5; col.5, ll.45-53].

14.9. Cheung discloses the compatibility between the resource and the controller is such that the slave clock is synchronized to within one clock cycle of the master clock [col.4, ll.37-41; set the precision values such as Q and restrict the transmission times appropriately].

14.10. Cheung discloses a method for synchronizing a controller [master or process B] and resource [slave or process A] clocks [col.1, ll.8-12].

14.11. Cheung discloses the method comprising saving a first value [time T] of the slave clock [col.4, ll.6-7].

14.12. Cheung discloses the method comprising sending a message from the resource to the controller via the network to request the value [time U] saved for the master clock [col.2, ll.66-67; col.4, ll.8-10].

14.13. Cheung discloses the method comprising sending the value saved for the master clock from the controller to the resource via the network [col.2, l.67 to col.3, l.2; col.4, ll.11-12].

14.14. Cheung discloses the method comprising receiving the value saved for the master clock at the resource [col.2, l.2; col.4, l.12].

14.15. Cheung discloses the method comprising saving a second value of the slave clock [time V] in the resource [col.2, ll.2-3; col.4, ll.13-14].

14.16. Cheung discloses the method comprising subtracting the first value [time T] from the second value [time V] to determine a slave clock difference value [V-T] [col.4, ll.30-32].

14.17. Cheung discloses the method comprising adding the difference value [V-T] to the value saved for the master clock [U] to determine a synchronized value for [U+V-T] the slave clock and setting the slave clock to the synchronized value [col.4, ll.37-41; Q=0].

14.18. Cheung discloses the method comprising subtracting the value saved for the slave clock [time T] from the value saved for the master clock [time U] to determine an error value between the slave clock and the master clock [U-T] and using the error value in an adjustment algorithm to adjust the slave clock to be synchronized with the master clock [col.4, ll.37-41; utilize V and Q in algorithm].

14.19. Cheung discloses the method wherein the periodic interval for performing the steps [a through g in application] during steady state operation of the document processing system is about two seconds [col.4, ll.37-41; with Q=0 and ignoring calculation time assumed to be

insignificant, focus on the more significant transmission time if that be the case so that the algorithm involving Q, V, and T would yield 2].

14.20. Cheung teaches that the advantage of using the round trip clock synchronization scheme as taught by Cristian can provide further precision tuning [col.3, ll.23-31] and enhance the accuracy of the network synchronization results [col.2, ll.47-52].

14.21. Shinoda et al., U.S. Patent 6675249, hereinafter Shinoda, discloses an information processing system with a processor for determining the compatibility of a plurality of clocks [col.7, ll.49-50].

14.22. Lackman et al., U.S. Patent 6343351, hereinafter Lackman, discloses a data processing system providing hard real-time service [col.3, ll.24-32].

14.23. Lackman teaches the advantage of providing hard real-time service is the prevention of catastrophic results in critical systems due to data loss [col.3, ll.29-32].

14.24. Einbinder et al., U.S. Patent 6704302, hereinafter Einbinder, discloses a 10 base T network for connecting workstations [col.3, ll.4-19].

14.25. Kurd et al., U.S. Patent 6320424, hereinafter Kurd, discloses the synchronization of a clock during steady state operation [col.8, ll.10-12; col.9, ll.20-24].

Re Claim 2

15. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Shimoda.

16. In re claim 2, Yamanaka discloses each and every limitation of the claim, as discussed above in reference to claim 1. Yamanaka did not discuss the use of the resource processor for determining the compatibility of the slave clock with the master clock. Shimoda teaches a

processor for determining the compatibility of a plurality of clocks [finding 14.21] in order to provide synchronization. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the processor taught by Shimoda for determining the compatibility of the slave clock with the master clock in the resource circuitry disclosed by Yamanaka as the processor taught by Shimoda is a known device for use in determining the compatibility between two values suitable for use as the processor of Yamanaka. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a mechanism for determining the compatibility between the two clocks for synchronization.

Re Claims 4 and 8

17. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Lackman.

18. In re claim 4, Yamanaka discloses each and every limitation of the claim, as discussed above in reference to claim 3. Yamanaka did not discuss the use of the compatibility between the resource and the controller to provide hard real-time service. Lackman teaches a data processing system providing hard real-time service [finding 14.22] to avoid catastrophic results due to data loss within a limited time frame [finding 14.23]. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka and Lackman before him at the time the invention was made, to modify the clock synchronization system disclosed by Yamanaka to include the hard real-time service as taught by Lackman, in order to provide a hard real-time clock synchronization system [e.g., information from CPU 10 to CPU 20 must be received in a "fresh" state of no older than an X amount of clock cycles in order for system to function properly]. One of ordinary skill in the art would have been motivated to make such a

combination in order to provide a mechanism for ensuring the safety of the system with critical operations that need to be serviced within a limited time frame.

19. As to claim 8, see finding 14.1 and discussion above in reference to claim 4.

Re Claim 12

20. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Einbinder.

21. In re claim 12, Yamanaka discloses each and every limitation of the claim, as discussed above in reference to claim 6. Yamanaka did not disclose expressly the use of a 10 base T network for interconnecting the resources and the controller. Einbinder teaches a 10 base T network for interconnecting nodes in a network to take advantage of the timing margins [finding 14.24]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the 10 base T network as taught by Einbinder to connect the resources and controller disclosed by Yamanaka as the 10 base T taught by Einbinder is a known connecting device for use in the system of Yamanaka. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a mechanism for interconnecting the resources and controller with controllable timing margins for synchronization purposes.

Re Claims 5, 9, and 13-20

22. Claims 5, 9, and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Cheung.

23. In re claim 5, Yamanaka discloses each and every limitation of the claim, as discussed above in reference to claim 3. Yamanaka did not discuss the detail of the compatibility between the resource and the controller to be such that the slave clock is synchronized to within one clock

cycle of the master clock. Cheung teaches a system for synchronizing a master and slave clocks [finding 14.7], wherein the compatibility between the resource and the controller is such that the slave clock is synchronized to within one clock cycle of the master clock [finding 14.9] in order to avoid problems for practical use [finding 14.6]. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka and Cheung before him at the time the invention was made, to modify the system taught by Yamanaka to include the synchronization mechanism as taught by Cheung, in order to obtain the compatibility between the resource and the controller such that the slave clock is synchronized to within one clock cycle of the master clock. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to synchronize the clocks within a range and avoid problems for practical use.

24. As to claim 9, see finding 14.1 and discussion above in reference to claim 5.

25. In re claim 13, Yamanaka discloses each and every limitation of the claim [findings 5.2-5.4 and 14.1-14.5]. Yamanaka did not address how the resource can improve the accuracy of the synchronization. Cheung teaches a system for synchronizing a master and slave clocks [finding 14.7]. Thus, Cheung teaches a system similar to that of Yamanaka. Cheung further teaches the steps the resource may take to synchronize its clock with the controller's master clock [findings 14.10-14.17] in order to increase the accuracy of the synchronization [finding 14.20]. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka and Cheung before him at the time the invention was made, to modify the system taught by Yamanaka to include the synchronization mechanism as taught by Cheung, in order to provide a way for the resource to increase the accuracy of synchronization. One of ordinary skill in the art

would have been motivated to make such a combination as it provides a way to increase the accuracy of the synchronization.

26. As to claim 14, see finding 14.1 and discussion above in reference to claim 13.

27. In re claim 15, Yamanaka discloses each and every limitation of the claim [findings 5.2-5.4 and 14.1-14.5]. Yamanaka did not address how the resource can improve the accuracy of the synchronization. Cheung teaches a system for synchronizing a master and slave clocks [finding 14.7]. Thus, Cheung teaches a system similar to that of Yamanaka. Cheung further teaches the steps the resource may take to synchronize its clock with the controller's master clock [findings 14.10-14.14 and 14.18] in order to increase the accuracy of the synchronization [finding 14.20]. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka and Cheung before him at the time the invention was made, to modify the system taught by Yamanaka to include the synchronization mechanism as taught by Cheung, in order to provide a way for the resource to increase the accuracy of synchronization. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase the accuracy of the synchronization.

28. As to claim 16, see discussion above in reference to claim 5.

29. As to claim 17, see finding 14.25.

30. As to claim 18, see finding 14.19.

31. As to claim 19, see discussion above in reference to claim 14.

32. As to claim 20, see discussion above in reference to claim 9.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Bedard et al., U.S. Patent 4644498, discloses a fault-tolerant real time clock system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (703) 305-8580. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703) 308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
June 3, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER ~~3600~~ 2100